AMENDMENTS TO THE SPECIFICATION

The entire specification is presented:

BACKGROUND OF INVENTION

Field of the Invention

The invention relates to a package structure, and more particularly, to a package structure capable of achieving greater reliability and production yield.

Description of the Prior Art

In the semiconductor industry, the production of integrated circuits is generally divided into two stages: integrated circuit manufacturing and integrated circuit packaging. The manufacturing of integrated circuit includes processes such as wafer manufacturing, circuit design, photomask manufacturing, and wafer dicing. Integrated circuit packaging on the other hand, includes processes such as wire bonding or flip chip assembly for electrically connecting a circuit chip to a substrate or a lead frame.

As the demand of smaller, more functional and complex PDAs, cellular phones, CPUs, and memory modules increases each day, the development of semiconductors also moves toward a direction of higher density packaging. Among many popular package structures, a flip chip (FC) structure with the characteristics of rapid cooling, low inductance, multi-terminal, and small size has been used most commonly in favor of others. In general, a flip chip package involves formation of a plurality of bumps on a chip and the addition of a layer of solder paste on the lead frame. The chip is then attached to the lead frame by melting the paste via a reflow process. Essentially, this type of package structure has already been disclosed in United States Patent No. 6,661,087. Nevertheless, the reflow process often causes the melting-state chip bumps and the solder paste to travel on the lead frame, which eventually causes the chip to move

away from its original position and result in problems such as product failure or low production yields.

In the recent history of integrated circuit packaging, passive devices (i.e. electrical resistors, capacitors, or inductors) have often been used for applications requiring high frequency or various other electrical properties. In the past, passive devices have generally been placed on the surface of printed circuit boards (PCBs). However, in order to reduce the space occupied on the PCB, most passive devices today are integrated into the chip. Eventually, a system in a package (SiP) was formed to provide a high efficiency, low cost, and small size package design for the market.

In the SiP design, the solder paste is often used as a linking medium between the passive device and the lead frame. After being processed by a reflow process via high temperature, the melting solder paste readily bonds the passive device and the lead frame together. Nevertheless, the reflow process often causes the solder paste to travel on the lead frame and the passive device to shift from its original position and results in problems such as product failure or low production yield. Consequently, it becomes a critical matter for the package industry to actively look for a package structure design that is able to effectively prevent the solder paste from moving on the lead frame.

SUMMARY OF INVENTION

It is therefore an objective of the claimed invention to provide a package structure for solving the problems stated previously.

The present invention relates to a package structure. The package structure includes a lead frame having a plurality of leads, each of which includes a first recession, at least a ~~first device~~semiconductor chip, and a plurality of solder joints respectively positioned in the first recessions for connecting the ~~first device~~semiconductor chip to the

lead frame.

As the present invention includes a plurality of lead frame recessions for fixing each solder joints in place, the joints are likely to remain in its original position during the melting state of a reflow process, thereby significantly increasing the overall yield and reliability of the package structure.

These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a cross-section view of a package structure of the first embodiment of the present invention.

Fig. 2 is a top view of a lead frame from Fig. 1.

Fig. 3 is a cross-section view of a cross line 3-3' of the lead frame from Fig. 2.

Fig. 4 is schematic diagram of a package structure manufacturing method of the first embodiment of the present invention.

Fig. 5 is a cross-section view of a chip-sink-lacking package structure of the first embodiment of the present invention.

Fig. 6 is a top view of a package structure of the second embodiment of the present invention.

Fig. 7 is a cross-section view of a cross line 6-6' of the package structure from Fig. 6.

DETAILED DESCRIPTION

Please refer to Fig. 1 to Fig. 3. Fig. 1 is a cross-section view of a package structure of the first embodiment of the present invention. Fig. 2 is a top view of a lead frame from Fig. 1 and Fig. 3 is a cross-section view of a cross line 3-3' of the lead frame from Fig. 2. As shown in Fig. 1, the package structure 10 includes a lead frame 12, at least a device 18 located on the lead frame 12, a plurality of solder joints 22 located between the lead frame 12 and the device 18, and a mold compound24 disposed around the device 18. As shown in Fig. 2 and Fig. 3, the lead frame 12 includes a die pad 14 for holding the device 18 and a plurality of leads 16, each of which contains a recession 16a. In addition, as indicated in Fig. 1, the device 18 includes a semiconductor die with a active surface and a plurality of bumps 20 are formed on active surface of semiconductor die, in which each of the bumps 20 is connected to each recession 16a via the solder joint 22. In general, the lead frame 12 comprises metal material (such as copper alloy or iron alloy), and the solder joint 22 comprises tin or tin alloy. In order to increase the defense mechanism of the device 18 to water vapor and oxidation, the mold compound 24 is composed of high polymeric material such as epoxy. The die pad 14 is connected to the device 18 to serve as a heat sink for radiating heat. Furthermore, a ground pad (not shown) can also be added on top of the die pad 14 to electrically connect to a ground connector (not shown) of the device 18.

Please refer to Fig. 4. Fig. 4 is schematic diagram of a package structure manufacturing method of the first embodiment of the present invention. As shown in Fig. 4, a plurality of bumps 20 are preformed on active surface of the semiconductor die . A lead frame 12 includes a plurality of leads 16 and a recession 16a is formed on each of the lead 16 via etching and is filled up by solder paste via printing.

Thereinafter, the device 18 is connected to the lead frame 12 to place each of the bumps 20 within the corresponding recession 16a. Next, a reflow process is performed for melting the solder paste 22b and forming the solder joint 22 as shown in Fig. 1 between the device 18 and the lead frame 12. Eventually, a mold compound 24 is

disposed around the semiconductor die 18 for protection. In general, the solder paste 22b is composed of tin or tin alloy. In order to prevent the semiconductor device 18 from any shift in position, the size of each of the recession 16a will need to be larger than each of the bumps 20. Depending on product specification and manufacturing need, the device 18 can also be fixed directly onto the lead 16 by omitting the die pad 14, as shown in Fig. 5. Fig. 5 is a cross-section view of a chip-sink-lacking package structure of the first embodiment of the present invention.

As noted previously, the metal lead frame 12 of the present invention includes a plurality of recessions 16a for fixing each bump 20 in place. In other words, the recessions 16a are formed within the lead 16, such that the solder joint and recession combination functions to provide a means of support for the semiconductor device 18 thereby preventing the device from any movement during reflow processes. As a result, the present invention is able to ~~preventing bump 20 and solder paste 22b from shifting positions during the reflow process,~~ maintain~~ing~~ the electrical performance of the semiconductor device 18~~,~~ and ultimately increase~~ing~~ the overall yield and reliability of the package structure 10.

Please refer to Fig. 6 and Fig. 7. Fig. 6 is a top view of a package structure of the second embodiment of the present invention and Fig. 7 is a cross-section view of a cross line 6-6' of the package structure from Fig. 6. As shown in Fig. ~~5~~6, the package structure 30 includes a lead frame 32, at least a device 40 located on the lead frame 32, and a plurality of passive devices 46 located on the lead frame 32. The lead frame 32 further includes a die pad 34 for holding the device 40 and a plurality of leads 36 and 38. The device 40 is connected to each lead 36 via a lead wire 42. Conceptually, the device 40 can be connected to the lead 38 of the passive device 46 via a lead wire. As shown in Fig. 6 and Fig. 7, the passive device 46 includes a plurality of outputs 48, in which each of the outputs 48 is respectively positioned in the recession 38a and connected to the lead 38 via a plurality of solder joints 50. ~~each of the leads 38 further comprises a recession~~

~~38a that connects to the output 48 of each of the passive devices 46 via a solder joint 50.~~ ~~In general~~ Preferably, the device 40 is a semiconductor die and each of the passive devices 46 is an electrical resistor, a capacitor, or an inductor. The lead frame 32 is composed of metal (such as copper alloy or iron alloy) and the solder joint 50 is composed of tin or tin alloy. The package structure 30 also includes a mold compound (not shown) disposed around the semiconductor die 40 and each of the passive devices 46 for protecting the devices.

Essentially, by connecting the passive device 46 to the recessions 38a of the lead 38 via outputs 48 and solder joints 50, the present invention is able to prevent the passive device 46 from any movement during reflow process. ~~In essence, the metal lead frame 32 includes a plurality of recessions 38a for preventing the melting state solder joint 50 from shifting positions during a reflow process,~~ thereby increasing the overall yield and reliability of the package structure 30. Preferably, the~~The~~ manufacturing technique of the package structure shown in Fig. 7 is ~~essentially~~ the same as the one in Fig. 4. As shown in Fig. 6, the semiconductor die 40 is electrically connected to each of the leads 36 via wire bonding while the passive device 46 is connected to the recessions 38a of the lead 38 by utilizing the outputs 48 and solder joints 50. Nevertheless, ~~an~~ alternative methods of assembling a flip chip package can also be used to electrically connect the chip to each of the lead.

In contrast to prior art technology, by utilizing the combination of recessions 16a and 38a and the solder joints 22 and 50 within the lead frame 12 and 32, the present invention is able to prevent the semiconductor chip and passive devices from any movement during reflow processes, ~~the lead frame 12 and 32 of present invention includes the recessions 16a and 38a, hence the solder joint 22 and 50 can be well maintained in its original position during a reflow process,~~ thereby increasing the overall yield and reliability of the package structure 10 and 30.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.